



Date: July.28, 2011

ATD-4950

TENTATIVE

TECHNICAL DATA**VVF42F118G00****CONTENTS**

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**RECORD OF REVISION**

Date	The upper section : Previous revision The lower section : New revision		Summary
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**DESCRIPTION**

The following specifications are applied to the following IPS-Pro-TFT LCD module.

Product Name : VVF42F118G00

General Specifications

Effective display area	: (H) 930.24 × (V) 523.26	(mm)
Number of pixels	: (H) 1,920 × (V) 1,080	(pixels)
Pixel pitch	: (H) 0.4845 × (V) 0.4845	(mm)
Color pixel arrangement	: R+G+B vertical stripe	
Display mode	: Transmissive mode Normally black mode	
Top polarizer type	: Semi-Glare	
Number of colors	: 1,073,741,824	(colors)
External dimensions	: Typ. (H) 966.64 × (V) 562.76 × (T) (3)	(mm)
Weight	: Typ. 2,200	(g)

1. ABSOLUTE MAXIMUM RATINGS

1.1 Environmental Absolute Maximum Ratings

ITEM	Operating		Storage		UNIT	NOTE
	Min.	Max.	Min.	Max.		
Temperature	0	40	-20	60	°C	1),5),6)
Humidity	2)		2)		%RH	1)
Vibration	-	4.9(0.5 G)	-	9.8(1.0G)	m/s ²	3)
Shock	-	29.4(3 G)	-	196(20G)	m/s ²	4),5)
Corrosive Gas	Not Acceptable		Not Acceptable		-	
Illumination at LCD Surface	-	50,000	-	50,000	1x	

- Note 1) Temperature and Humidity should be applied to the glass surface of a IPS-Pro TFT LCD module, not to the system installed with a module.
- 2) $T_a \leq 40^\circ\text{C}$ ······ Relative humidity should be less than 85 %RH max. Dew is prohibited.
 $T_a > 40^\circ\text{C}$ ······ Relative humidity should be lower than the moisture of the 85 %RH at 40°C .
- 3) Frequency of the vibration is between 15 Hz and 100 Hz. (Remove the resonance point) 1 hour.
- 4) Pulse width of the shock is 10 ms.
- 5) Long operation under low temperature may cause some portion of display area to be reddish for several minutes after turning on the product.
 However, it does not affect the characteristics and reliability of the product.
- 6) Environmental Absolute Maximum Ratings is Based on IPS Alpha Technology TFT standard module.
 Leave TFT open cell alone, this environmental ratings can't be guaranteed. The users have a responsibility in considering ability of other parts of TFT module and TFT module process.

1.2 Electrical Absolute Maximum Ratings

(1)TFT-LCD module

GND = 0 V

ITEM	SYMBOL	Min.	Max.	UNIT	NOTE
Source Driver Analog Power Supply	AVDD	-0.3	18	V	
Source Driver Analog Power Supply-1	AVDDMH	-0.3	AVDD	V	
Source Driver Analog Power Supply-2	AVDDML	-0.3	AVDD	V	
Driver Logic Power Supply	VDD	-0.3	4.0	V	
Gate Driver Power Supply	VON	-0.3	VOFF+44	V	
Gate Driver Ground	VOFF	-22	0.3	V	
Gate Driver Power Supply Range	VON-VOFF	-0.3	45	V	
Gamma Corrected Power Supply	VREF1~5	AVDD-10.5	AVDD+0.3	V	
	VREF6	AVDD-10.5	10.5	V	
	VREF8~12	-0.3	10.5	V	
Input Voltage for logic	V _I	-0.3	VDD + 0.3	V	1)
Electrostatic Durability	V _{ESD0}	± 100		V	2),3)

- Note 1) It is applied to pixel data sigi
- 2) Discharge Coefficient : 200 pF - 250 Ω, Environmental : 25 °C - 70%RH
- 3) It is applied to I/F connector pins.

1.3 Environmental Absolute Ratings of TFT open cell

Storage Condition : With shipping package

Storage temperature range : 25±5 °C

Storage humidity range : 50±10%RH

Shelf life : a month

2. INITIAL OPTICAL CHARACTERISTICS

The following optical characteristics are measured under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted.

The optical characteristics should be measured in a dark room or equivalent state.

Measuring equipment : CS-1000A, or equivalent

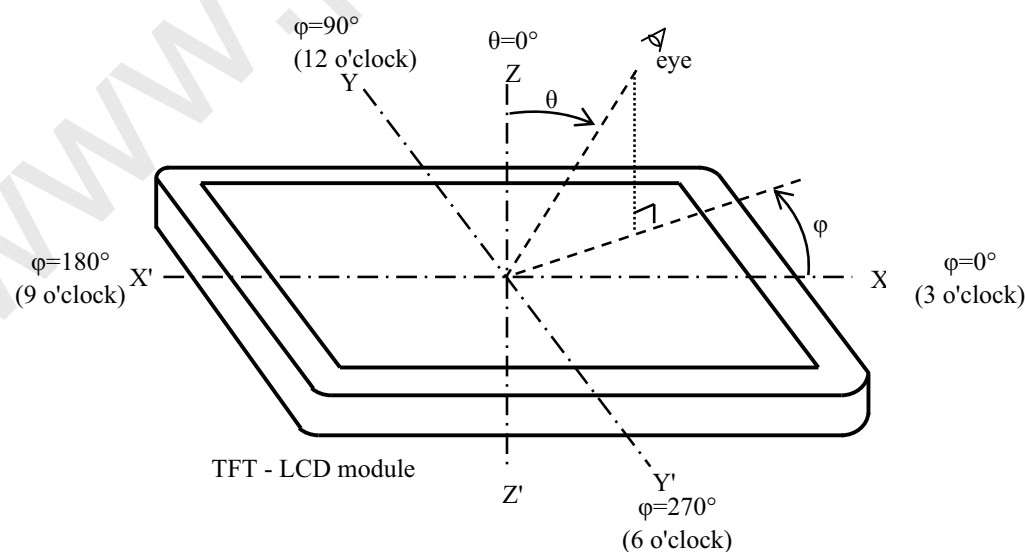
Ambient Temperature =25 °C , $V_{DD}=12.0\text{ V}$, $f_V=120\text{ Hz}$,

$I_{fc}=68\text{ mA/string}$ (On-duty=100%)

Light source is backlight of Panasonic Liquid Crystal Display Co.,Ltd. TFT standard module.

ITEM		SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT	NOTE
Contrast ratio		CR	$\theta = 0^\circ$ 1)	800	1400	-	-	2)
Response time	Rise	ton		-	10	20	ms	3)
	Fall	toff		-	8	16	ms	3)
Brightness of white		Bwh		350	450	-	cd/m ²	
Brightness uniformity		Buni		-	-	40	%	4)
Color chromaticity (CIE)	Red	x		0.560	0.590	0.620	-	【Gray scale =1023】
		y		0.305	0.335	0.365		
	Green	x		0.310	0.340	0.370		
		y		0.570	0.600	0.630		
	Blue	x		0.125	0.155	0.185		
		y	0.035	0.065	0.095			
	White	x	0.250	0.280	0.310			
		y	0.253	0.283	0.313			
Variation of color position (CIE)	Red	Δx	$\theta = 50^\circ$ $\varphi = 0^\circ, 90^\circ, 180^\circ, 270^\circ$ 1)	-	-	0.04	-	5) 【Gray scale =1023】
		Δy		-	-	0.04		
	Green	Δx		-	-	0.04		
		Δy		-	-	0.04		
	Blue	Δx		-	-	0.04		
		Δy		-	-	0.04		
	White	Δx		-	-	0.04		
		Δy		-	-	0.04		
Contrast ratio at 89 °		CR89	6)	10	-	-	-	Estimated value

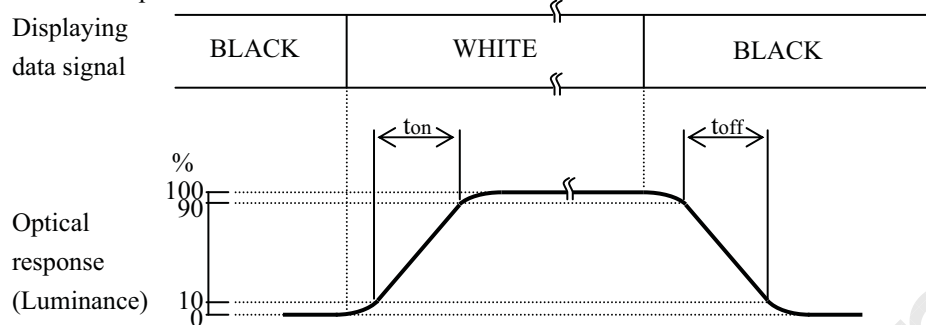
Note 1) Definition of viewing angle



Note 2) Definition of contrast ratio (CR)

$$CR = \frac{(\text{Luminance at displaying WHITE})}{(\text{Luminance at displaying BLACK})}$$

3) Definition of response time



4) Definition of brightness uniformity

Display pattern is white (1023 level). The brightness uniformity is defined as the following equation. Brightness at each point is measured, and average, maximum and minimum brightness is calculated.

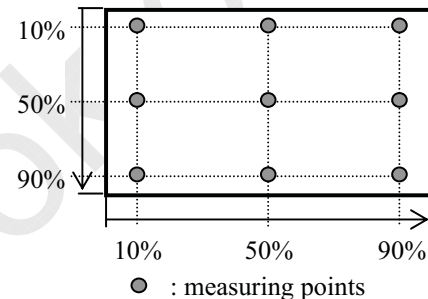
$$B_{uni} = \frac{|B_{max} \text{ or } B_{min} - B_{ave}|}{B_{ave}} \times 100$$

where, B_{max} = Maximum brightness

B_{min} = Minimum brightness

B_{ave} = Average brightness

$$B_{ave} = \frac{\sum_{k=1}^9 (B(k))}{9}$$



5) Variation of color position on CIE

Variation of color position on CIE is defined as difference between colors at $\theta = 0^\circ$ and at $\theta = 50^\circ$ & $\phi = 0^\circ$, 90° , 180° , 270° .

6) Contrast ratio at 89°

Evaluation conditions are on horizontal & vertical axis

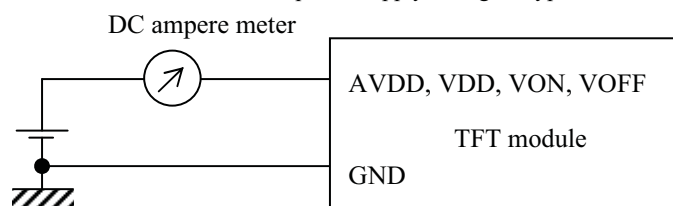
3. ELECTRICAL CHARACTERISTICS

3.1 TFT-LCD module

Ta = 25 °C , GND = 0 V

ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Source Driver Analog Power Supply Voltage	AVDD	12.286	12.586	12.886	V	
Ripple voltage of AVDD	Vrip_avdd	-	-	300	mV	1), 3)
Source Driver Analog Power Supply Voltage-1	AVDDMH	VREF6+0.2	6.70	6.85	V	
Ripple voltage of AVDDMH	Vrip_avddmh	-	-	300	mV	1), 3)
Source Driver Analog Power Supply Voltage-2	AVDDML	5.85	6.00	VREF6-0.2	V	
Ripple voltage of AVDDML	Vrip_avddml	-	-	300	mV	1), 3)
Driver Logic Power Supply Voltage	VDD	2.4	2.5	2.6	V	
Ripple voltage of VDD	Vrip_vdd	-	-	150	mV	1), 3)
Gate Driver Power Supply Voltage	VON	29.0	30.5	32.5	V	
Ripple voltage of VON	Vrip_von	-	-	500	mV	1), 3)
Gate Driver Ground Voltage	VOFF	-6.35	-5.8	-5.25	V	
Ripple voltage of VOFF	Vrip_voff	-	-	200	mV	1), 3)
Input High Voltage for logic	VIH1	0.8VDD	-	VDD	V	2)
Input Low Voltage for logic	VIL1	0	-	0.2VDD	V	2)
Common Plate Voltage	VCOM	-	4.548	-	V	
Ripple voltage of VCOM	Vrip_vcom	-	-	200	mV	1), 3)
Source Driver Analog Power Supply Current	IADD	-	200	300	mA	1)
Source Driver Analog Power Supply-1 Current	IADDH	-	175	250	mA	1)
Source Driver Analog Power Supply-2 Current	IADDL	-250	-175	-	mA	1)
Driver Logic Power Supply Current	IDD	-	60	100	mA	1)
Gate Driver Power Supply Current	ION	-	6.0	10	mA	1)
Gate Driver Ground Current	IOFF	-10.0	-6.0	-	mA	1)
Gamma Corrected Power Supply Voltage 1	VREF1	-	12.193	-	V	
Gamma Corrected Power Supply Voltage 2	VREF2	-	10.718	-	V	
Gamma Corrected Power Supply Voltage 3	VREF3	-	9.353	-	V	
Gamma Corrected Power Supply Voltage 4	VREF4	-	8.690	-	V	
Gamma Corrected Power Supply Voltage 5	VREF5	-	8.186	-	V	
Gamma Corrected Power Supply Voltage 6	VREF6	-	6.354	-	V	
Gamma Corrected Power Supply Voltage 8	VREF8	-	4.426	-	V	
Gamma Corrected Power Supply Voltage 9	VREF9	-	3.945	-	V	
Gamma Corrected Power Supply Voltage 10	VREF10	-	3.269	-	V	
Gamma Corrected Power Supply Voltage 11	VREF11	-	1.893	-	V	
Gamma Corrected Power Supply Voltage 12	VREF12	-	0.393	-	V	
Ripple voltage of VREF	Vrip_VREF	-	-	200	mV	3), 4)

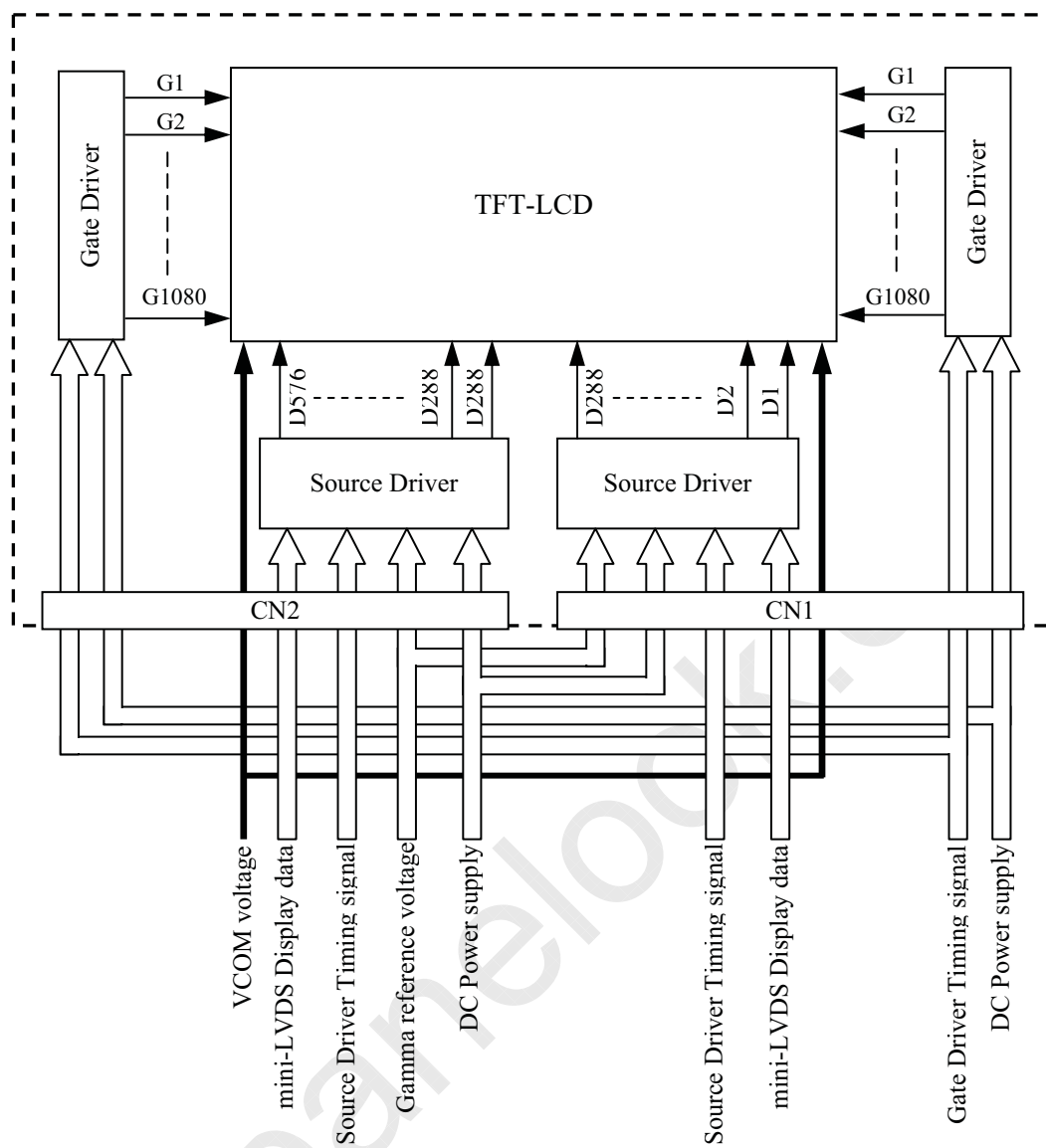
Note 1) fV=120.0Hz, fCLK=240.0MHz, each power supply voltage is typical condition and display pattern is white raster



- 2) It is applied to LP, POLR, POLL, CPV, DATA1 and DATA2 signal.
- 3) The above specification is defined at connector CN1 and CN2.
- 4) Display pattern is 128gray raster.

4. BLOCK DIAGRAM

4.1 TFT-LCD module



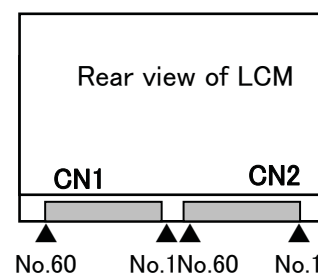
5. INTERFACE PIN ASSIGNMENT

5.1 TFT-LCD module

CN1:MOLEX 503366-6011

PIN No.	SYMBOL	DESCRIPTION	NOTE
1	VCOM-SL	Common Voltage	
2	LPL	Control Signal	
3	POLL	Control Signal	
4	N.C.	Non Connection	
5	VGMA12	Reference Voltage	
6	VGMA11		
7	VGMA10		
8	VGMA9		
9	VGMA8	Reference Voltage	
10	N.C.		
11	GND		
12	AVDD		
13	AVDD	Analog Voltage	
14	AVDDMH	Analog Voltage	
15	AVDDMH		
16	AVDDML	Analog Voltage	
17	AVDDML		
18	GND	GND(0V)	
19	LV7BL	Pixel Data	
20	LV7AL		
21	LV6BL	Pixel Data	
22	LV6AL		
23	GND	GND(0V)	
24	LV5BL	Pixel Data	
25	LV5AL		
26	LV4BL	Pixel Data	
27	LV4AL		
28	GND	GND(0V)	
29	CLKBL	Pixel Clock	
30	CLKAL		

PIN No.	SYMBOL	DESCRIPTION	NOTE
31	GND	GND(0V)	
32	LV3BL	Pixel Data	
33	LV3AL		
34	LV2BL	Pixel Data	
35	LV2AL		
36	GND	GND(0V)	
37	LV1BL	Pixel Data	
38	LV1AL		
39	LV0BL	Pixel Data	
40	LV0AL		
41	GND	GND(0V)	
42	VOFF	Reference Voltage	
43	VONL		
44	DATA2L	Control Signal	
45	DATA1L	Control Signal	
46	CPVL	Control Signal	
47	N.C.	Non Connection	
48	VGMA6	Reference Voltage	
49	VGMA5		
50	VGMA4		
51	VGMA3		
52	VGMA2		
53	VGMA1	GND(0V)	
54	GND		
55	GND		
56	VDD	Logic Voltage	
57	VDD		
58	GND	GND(0V)	
59	VCOM	Common Voltage	
60	VCOM		



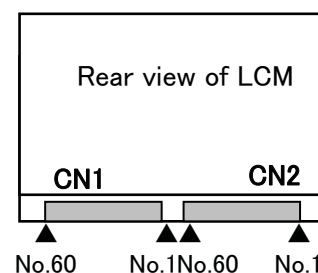
5. INTERFACE PIN ASSIGNMENT

5.1 TFT-LCD module

CN2:MOLEX 503366-6011

PIN No.	SYMBOL	DESCRIPTION	NOTE
1	N.C.	Non Connection	
2	LPR	Control Signal	
3	POLR	Control Signal	
4	N.C.	Non Connection	
5	VGMA12	Reference Voltage	
6	VGMA11		
7	VGMA10		
8	VGMA9		
9	VGMA8		
10	N.C.	Non Connection	
11	GND	GND(0V)	
12	AVDD	Analog Voltage	
13	AVDD		
14	AVDDMH	Analog Voltage	
15	AVDDMH		
16	AVDDML	Analog Voltage	
17	AVDDML		
18	GND	GND(0V)	
19	LV7BR	Pixel Data	
20	LV7AR		
21	LV6BR	Pixel Data	
22	LV6AR		
23	GND	GND(0V)	
24	LV5BR	Pixel Data	
25	LV5AR		
26	LV4BR	Pixel Data	
27	LV4AR		
28	GND	GND(0V)	
29	CLKBR	Pixel Clock	
30	CLKAR		

PIN No.	SYMBOL	DESCRIPTION	NOTE
31	GND	GND(0V)	
32	LV3BR	Pixel Data	
33	LV3AR		
34	LV2BR	Pixel Data	
35	LV2AR		
36	GND	GND(0V)	
37	LV1BR	Pixel Data	
38	LV1AR		
39	LV0BR	Pixel Data	
40	LV0AR		
41	GND	GND(0V)	
42	VOFF	Reference Voltage	
43	VONR		
44	DATA2R	Control Signal	
45	DATA1R	Control Signal	
46	CPVR	Control Signal	
47	N.C.	Non Connection	
48	VGMA6	Reference Voltage	
49	VGMA5		
50	VGMA4		
51	VGMA3		
52	VGMA2		
53	VGMA1		
54	GND	GND(0V)	
55	GND		
56	VDD	Logic Voltage	
57	VDD		
58	GND	GND(0V)	
59	VCOM	Common Voltage	
60	VCOM		



5.3 Correspondence between input data and display image

Display data of adjacent two pixel is latched during fore cycle of CLK.

B

G

R

(1,1)

(1,1)

(1,1)

Pixel : R0 - R7 : R (x,y)

G0 - G7 : G (x,y)

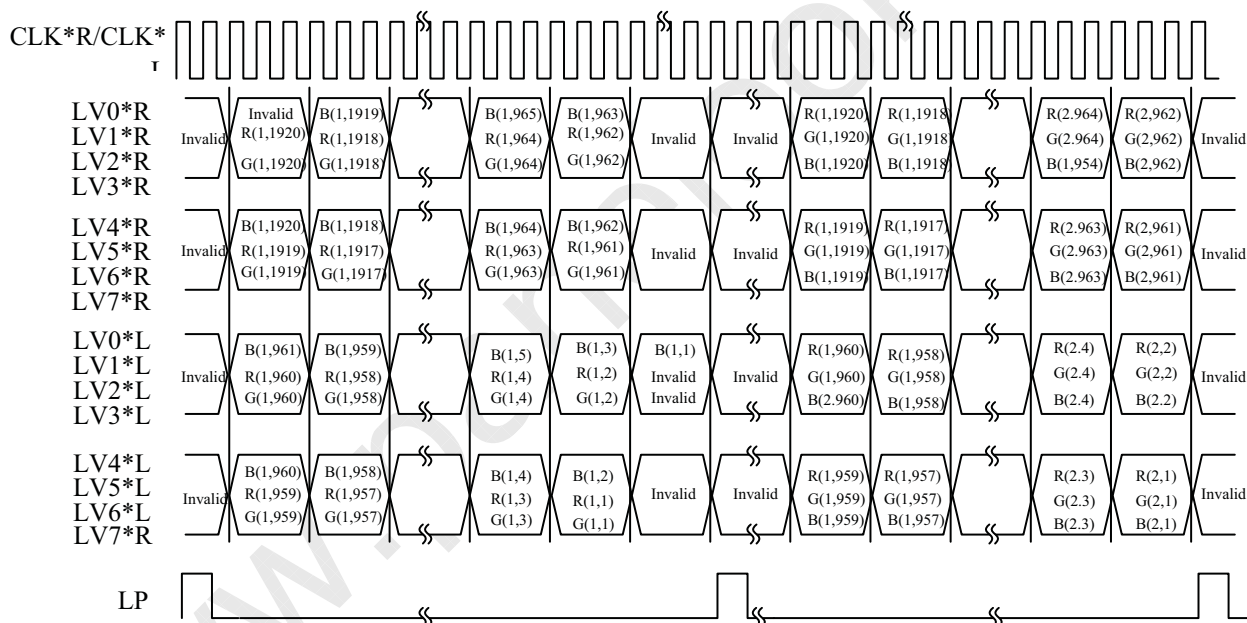
B0 - B7 : B (x,y)

upper

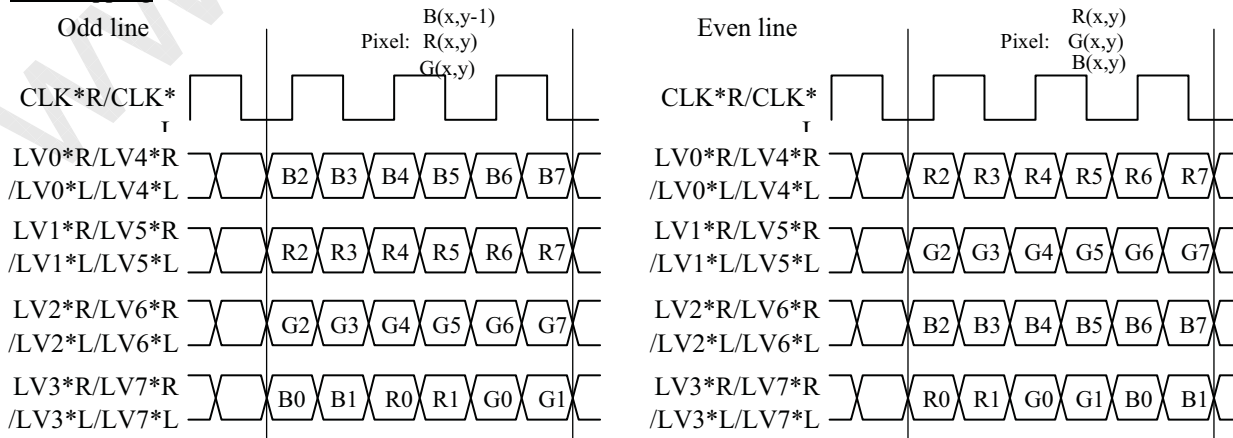
1 , 1	1 , 2	1 , 3	-----	1 , 959	1 , 960	1 , 961	1 , 962	-----	1 , 1919	1 , 1920
2 , 1	2 , 2	2 , 3	-----	2 , 959	2 , 960	2 , 962	2 , 962	-----	2 , 1919	2 , 1920
3 , 1	3 , 2	3 , 3	-----	3 , 959	3 , 960	3 , 963	3 , 962	-----	3 , 1919	3 , 1920
⋮	⋮	⋮		⋮	⋮	⋮	⋮		⋮	⋮
1080 , 1	1080 , 2	1080 , 3	-----	1080 , 959	1080 , 960	1080 , 961	1080 , 962	-----	1080 , 1919	1080 , 1920

lower

case:PCB in the panel upper part & Zigzag panel



data mapping





5. 4 Relationship between display colors and input signals

Input Color		Red Data								Green Data								Blue Data													
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0						
		MSB								LSB								MSB								LSB					
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0						
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1						
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1						
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1						
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0						
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1						
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:						
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0						
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0						
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:						
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:						
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0						
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0						
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0						
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0						
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:						
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:						
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0						
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1						

Note 1) Definition of gray scale :

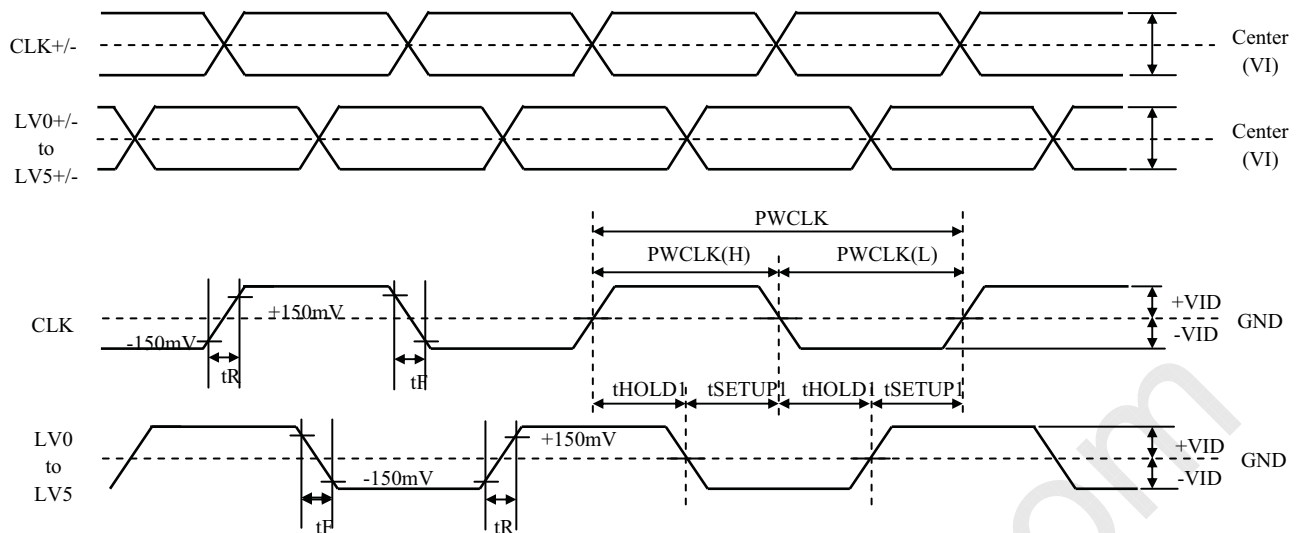
Color(n) · · · · Number in parenthesis indicates gray scale level.

Larger n correspondsto brighter level.

2) Data : 1 : High, 0 : Low

6. INTERFACE TIMING

6.1 mini-LVDS receiver timing



$$LVn=(LVn+)-(LVn-)\quad n=0\sim 5$$

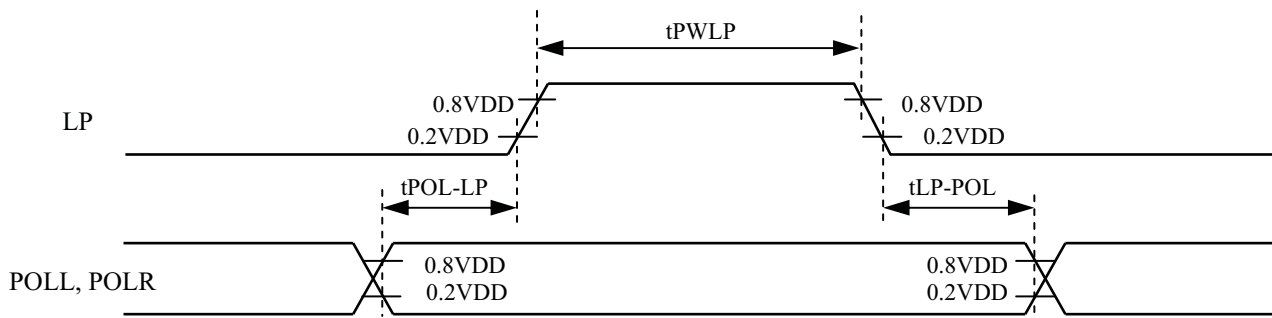
$$CLK=(CLK+)-(CLK-)$$

ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Clock period	PWCLK	4	4.17	4.3	ns	1)
Clock high level width	PWCLK(H)	1.7	2.085	-	PWCLK	1)
Clock Low level width	PWCLK(L)	1.7	2.085	-	PWCLK	1)
Data setup time	tSETUP1	0.65	1.04	-	ns	1)
Data hold time	tHOLD1	0.65	1.04	-	ns	1)
mini-LVDS rise time	tR	-	-	0.5	ns	1)
mini-LVDS fall time	tF	-	-	0.5	ns	1)
mini-LVDS differential voltage	VID	150	412	600	mV	1)
mini-LVDS common mode input voltage range	VI	0.5	0.8	1.1	V	1)

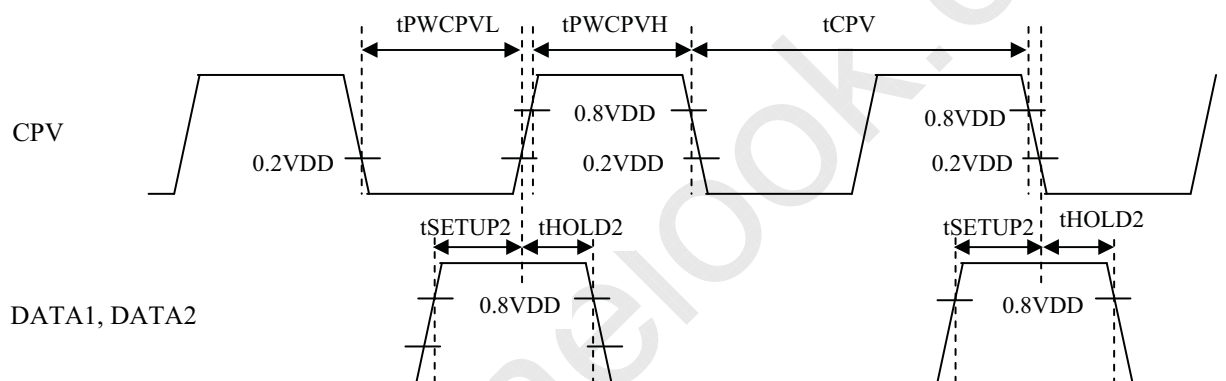
Notes 1) The above specification is defined at each Source Driver IC inputs.

6.2 Control signal timing

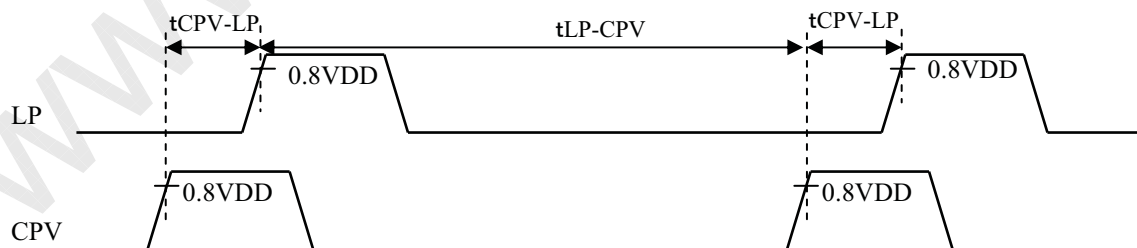
Notes 1) The following specification is defined at connector CN1.



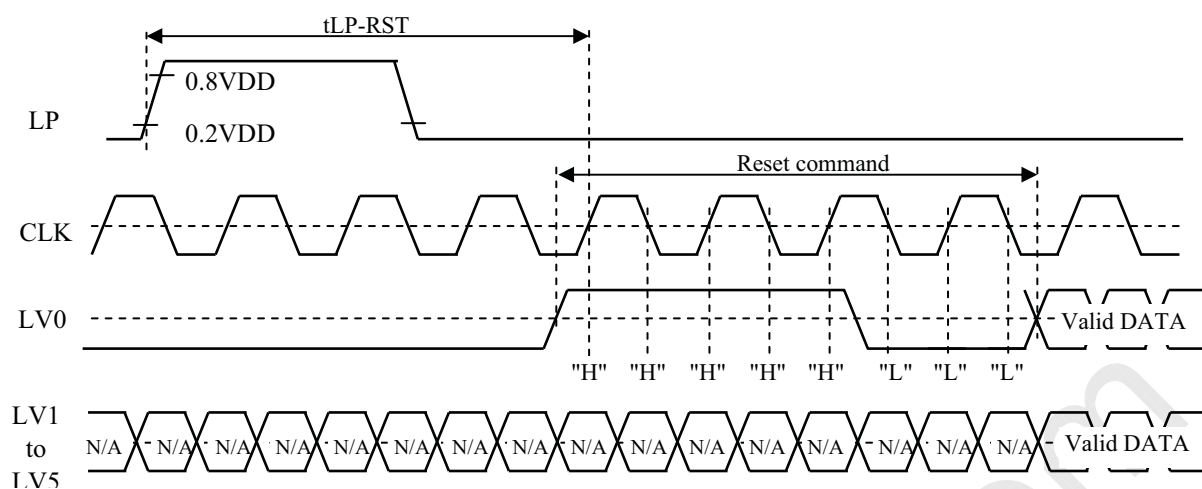
ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Latch clock high level width	t_{PWLP}	0.2	0.58	-	μs	
POL setup time	t_{POL-LP}	1.0	2.17	-	μs	
POL hold time	t_{LP-POL}	1.0	5.41	-	μs	



ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Gate shift clock period	t_{CPV}	7.46	7.58	7.88	μs	
Gate shift clock high level width	t_{PWCPVH}	0.7	0.88	1.0	μs	
Gate shift clock low level width	t_{PWCPVL}	-	6.6	-	μs	
Data setup time	t_{SETUP2}	0.3	0.44	-	μs	
Data hold time	t_{HOLD2}	0.3	0.44	-	μs	



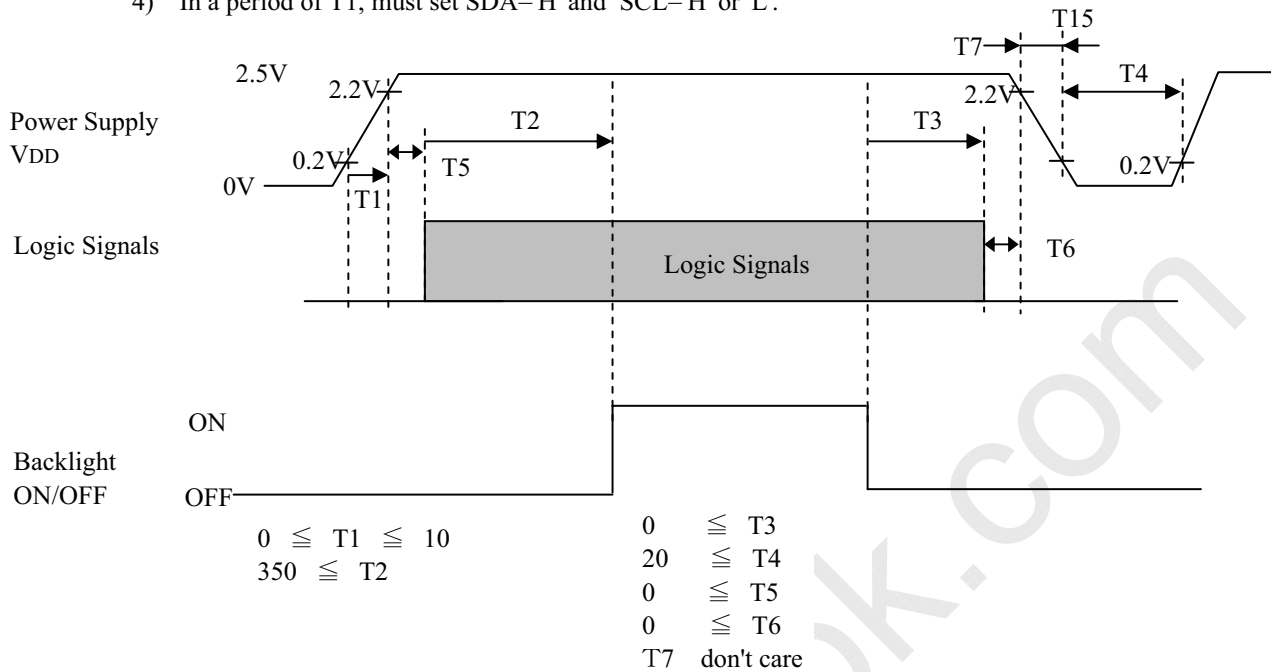
ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Gate delay time	t_{CPV-LP}	0.97	1.07	1.17	μs	
TFT charge time	t_{LP-CPV}	-	6.51	-	μs	



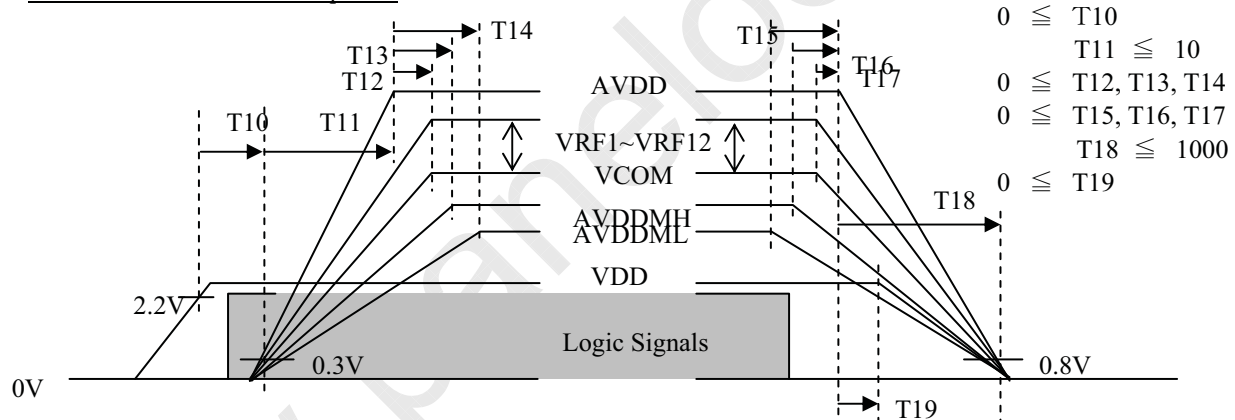
ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Reset input time	tLP-RST	24	-	-	PWCLK	

6.4 Timing between interface signals power supply

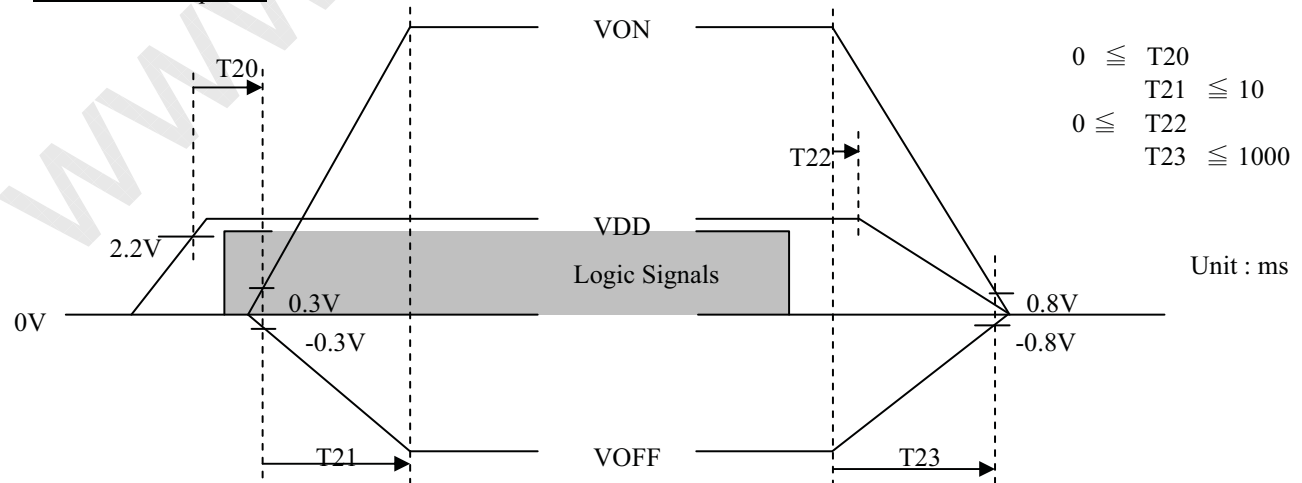
- Notes 1) The following specification is defined at connector CN1 and CN2.
 2) In the T10 and T11, the float equal to or less than 1.5V of AVDD is no object.
 3) In the T20 and T21, the float equal to or less than 1.5V of VON is no object.
 4) In a period of T1, must set SDA='H' and SCL='H' or 'L'.



Source Driver & VCOM Sequence



Gate Driver Sequence

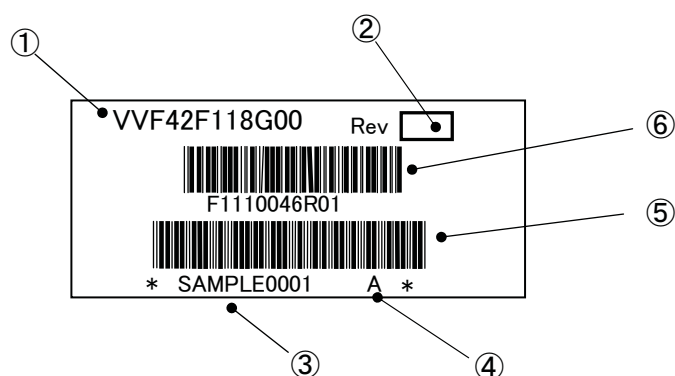


7. DESIGNATION OF LABEL

7.1 Label

The barcode label is pasted on each TFT open cell.

Users use this bar code label to write adjustment Vcom value and Liquid Crystal information to Tcon ROM which is specified by Panasonic Liquid Crystal Display Co.,Ltd.



Item	Description
①	Product Name
②	Rev. is the column for manufacturing convenience. A-Z except I and O may be written on this column.
③	Lot mark
④	Liquid crystal information Marker A : A, C, E, G, J, L, N, R Marker B : B, D, F, H, K, M, P, S
⑤	Bar code(③+④)
⑥	Bar code(IPSα inner management barcode)

7.2 Record of revision described on the label

Rev.BG = B grade cosmetic specifications

8. COSMETIC SPECIFICATIONS

8.1 Condition for cosmetic inspection

(1) Viewing zone

- a) The figure shows the correspondence between eyes (of inspector) and TFT-LCD module.

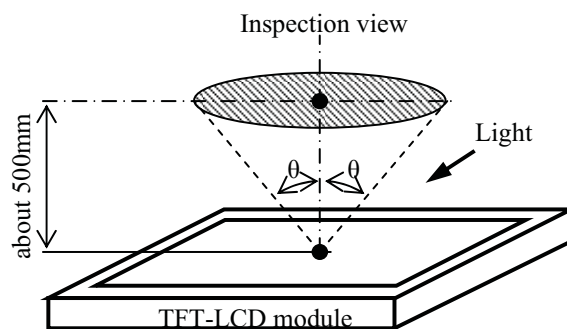
$\theta \leq 45^\circ$: when non-operating inspection

If $\theta \leq 5^\circ$: when operating inspection

- b) Inspection should be executed only from front side and only A-zone.

Cosmetic of B-zone and C-zone are ignore.

(refer to 9.2 Definition of zone)



(2) Environmental

- a) Temperature : 25 degrees

- b) Ambient light : about 700 lx and non-directive when operating inspection.

: about 1000 lx and non-directive when non-operating inspection.

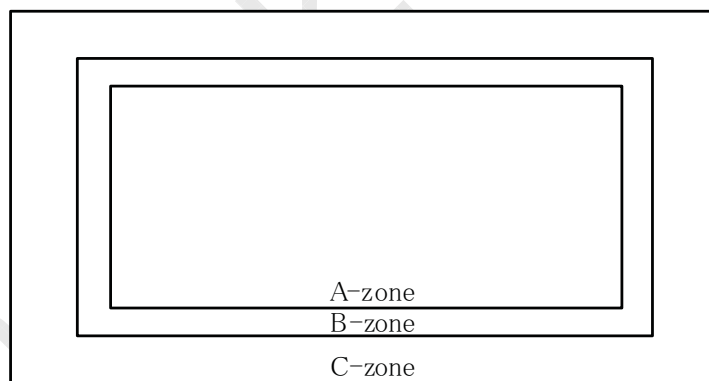
- c) Backlight : when non-operating inspection, backlight should be off .

8.2 Definition of zone

•A-zone : Display area (pixel area)

•B-zone : Area between A-zone and C-zone

•C-zone : Metallic bezel area



8.3 Cosmetic specifications

When displaying conditions are not stable (ex. at turn on or off), the following specifications are not applied.

	No	ITEM			Max. acceptable number	Unit	Note
					A-zone		
					Bgrade		
Operating inspection	1	Dot defect	Sparkle mode	1-dot	6	pcs	1),2),4)
				2-dots	2	Units	1),2),5)
				3-dots	1		
				Density	3	pcs/φ20mm	1),2),6)
				Total	7	pcs	1),2)
			Black mode	1-dot	15	pcs	1),3),4)
				2-dots	3	Units	1),3),5),10)
				3-dots	1		
				Density	4	pcs/φ20mm	1),3),6)
				Total	15	pcs	1),3)
			Total	21	pcs	1)	
	2	Line defect			Serious one is not allowed	-	-
	3	Uneven brightness					



	No	ITEM			Max. acceptable number	Unit	Note
					A-zone		
					Bgrade		
Operating inspection	4	Stain inclusion Line shape W : width (mm) { L : length (mm)}	W≤0.08	L : Ignore	Ignore	pcs	7)
			W≤0.25	L≤2.0	16		
				2.0<L≤4.0	8		
				L>4.0	0		
			W>0.25	-	(See dot shape)		
	5	Stain inclusion { Dot shape D : ave. dia (mm)}	D≤0.5		Ignore	pcs	7)
			D≤1.0		8		
			D>1.0		0		
	6	Scratch on polarizer { Line shape W : width (mm) L : length (mm)}	W≤0.15	L : Ignore	Ignore	pcs	8)
			W≤0.3	L≤20	10		
				L>20	0		
			W>0.3	-	0		
	7	Scratch on polarizer { Dot shape D : ave. dia (mm)}	D≤0.6		Ignore	pcs	8)
			D≤1.0		10		
			D>1.0		0		
Non operating inspection	8	Bubbles, peeling in polarizer {D : ave. dia (mm)}	D≤0.5		Ignore	pcs	8)
			D≤1.0		10		
			D>1.0		0		
	9	Wrinkles on polarizer			Serious one is not allowed.	-	-

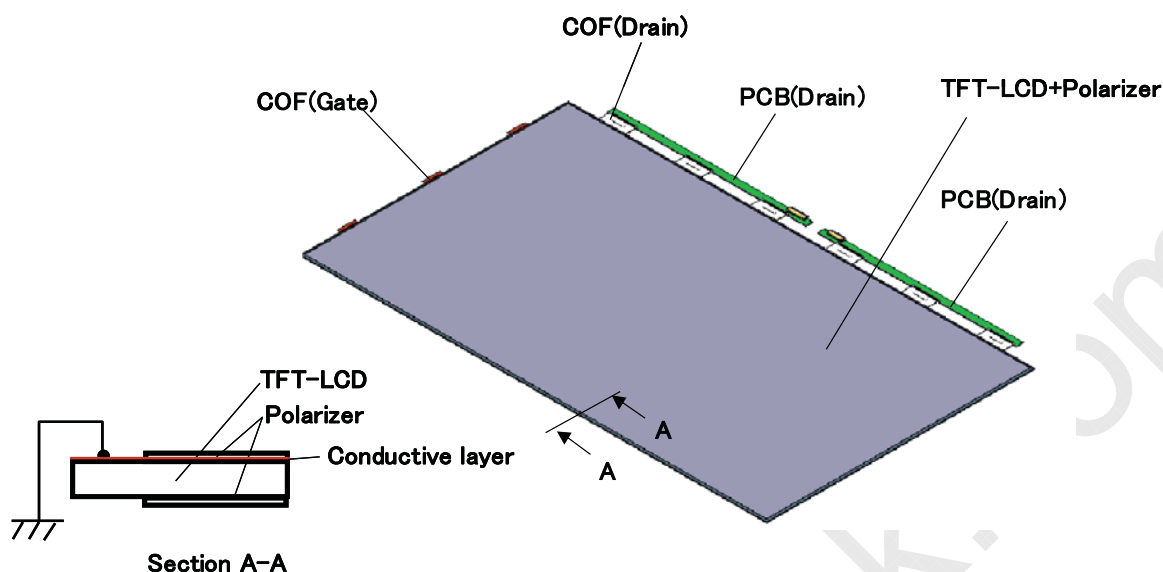
- Note
- 1) Dot defect : defect area $> 1/2$ dot
 - 2) Sparkle mode : brightness of dot is more than 30% at black. (visible to eye)
 - 3) Black mode : brightness of dot is less than 70% at white. (visible to eye)
 - 4) 1 dot : defect dot is isolated, not attached to other defect dot.
 - 5) N dots : N defect dots are consecutive. (N means the number of defects dots)
 - 6) Density : number of defect dots inside $\phi 20\text{mm}$
 - 7) Those stains which can be wiped out easily are acceptable.
 - 8) Polarizer area inside of B-zone is not applied.
 - 9) No major (serious) defects when viewed in gray scale mode.

9. PRECAUTION

Please pay attention to the followings when a TFT open cell is used, handled and mounted.

9.1 Recommendation of GND connection of TFT open cell

(1) Please connect LCD surface (front side) to GND for prevention of static charge.

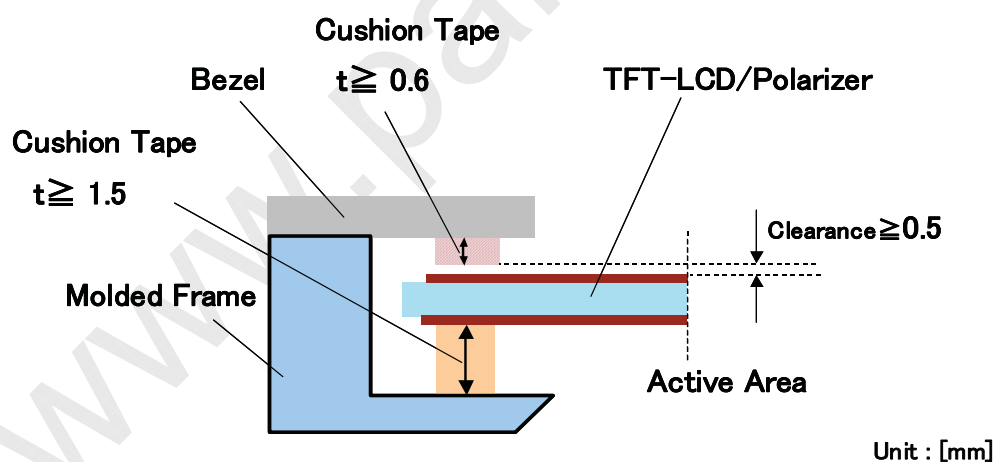


9.2 Recommendation of structure for supporting TFT-LCD Rim

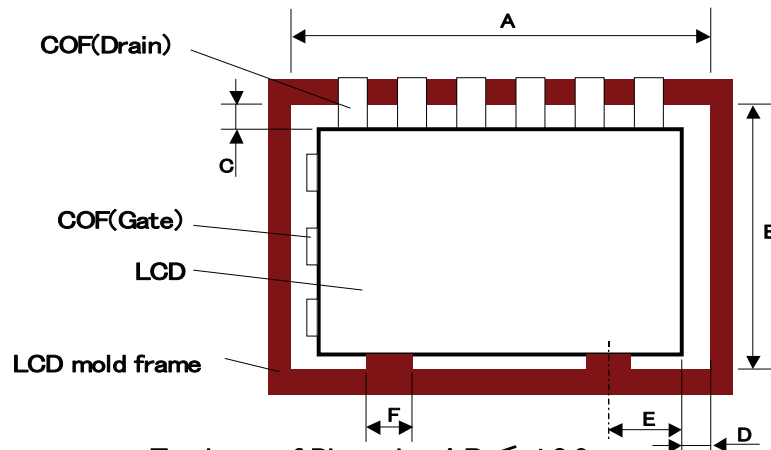
(1) When the LCD is applied by stress, it occurs abnormal image quality.

(It is confirmed visually especially in case of gray raster.)

The system shown on the drawing down below is recommended to maintain the LCD by cutting down the LCD stress.



(2)The dimension of mold frame and LCD is recommended as follows.



Tolerance of Dimension A,B $\leq \pm 0.6$

C = 0.8, D = 0.6

F=50~70 (32") E=120~130 (32")

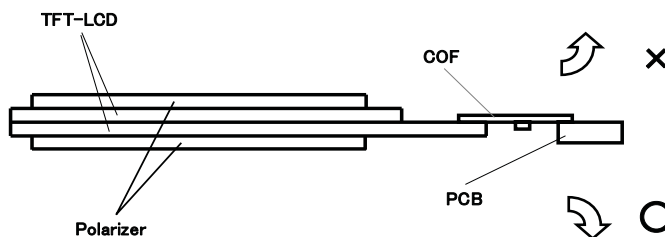
F=70~90 (37") E=145~155 (37")

Unit : [mm]

- (3)The wall of the mold frame should be laid on whole sides of the LCD as much as possible.
- (4)The holding space for the LCD should be maintained by the mold frame and the bezel.
- (5)Screw the mold frame to the lower frame at many places to keep flatness of LCD support area.
- (6)The mold frame should be the structure that is divided into four sides to keep flatness of LCD support area.
- (7)LCD support surface at lower side should smooth to cutting down the LCD stress.
(Put PET tape between LCD and support area, etc.)
- (8)At the time of ground connection, take a method that does not put a load to the LCD.
- (9)Use silicon rubber with hardness 20 for cushion to the mold frame side.
- (10)Use foaming cushion to Bezel side.
- (11)Flatness of the Bezel should be 0.5 which also should be the shape does not have partial changing points.
- (12)The bezel should be the structure that is divided into four sides and screwed from the upper side.
- (13)The surface of the cushion (the surface which attaches to the LCD) should be mat finishing or should put PET tape to avoid the LCD and the cushion from sticking together.

9.3 Precaution to handling and mounting

- (1)The polarizer on a TFT cell should carefully be handled due to its softness, and should not be touched, pushed or rubbed with glass, tweezers or anything than HB pencil lead. The surface of a polarizer should not be touched and rubbed with bare hand, greasy clothed or dusty clothes.
- (2) The surface of a polarizer should be gently wiped with absorbent cotton, chamois or other soft materials slightly contained petroleum benzene when the surface becomes dirty. Normal-hexane or Isopropyl alcohol as cleaning chemicals is recommended in order to clean adhesives which fix front/rear polarizers on a TFT cell. Other cleaning chemicals such as acetone, toluen and alcohol should not be used to clean adhesives because they cause chemical damage to a polarizer.
- (3)Saliva or water drops should be immediately wiped off. Otherwise, the portion of a polarizer and electronic parts may be deformed.
- (4)Applying upward bend to COF may cause a malfunction electrically and mechanically.



(5)Applying too much force and stress to PCB and COF may cause a malfunction electrically and mechanically.

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9.4 Precaution to operation

- (1) The ambient temperature near the operated cell and electronic parts should be satisfied with the ratings. Unless it meets the specifications, sufficient cooling system should be adopted to system.
- (2) The spike noise causes the mis-operation of a TFT open cell. The level of spike noise should be as follows:
-200mV<=over- and under- shoot of VDD<= +200mV
VDD including over- and under- shoot should be satisfied with the absolute maximum ratings.
- (3) Optical response time, luminance and chromaticity depend on the temperature of a TFT open cell.
- (4) Sudden temperature change may cause dew on and/or in the a TFT open cell. Dew males damage to a polarizer and/or electrical contacting portion. Dew causes fading of displayed quality.
- (5) Fixed patterns displayed on a TFT open cell for a long time may cause after-image. It will be recovered soon.
- (6) The TFT open cell has high frequency circuits. Sufficient suppression to electromagnetic interference should be done by system manufacturers. Grounding and shielding methods may be effective to minimize the interference.
- (7) Noise may be heard when a back-light is operated. If necessary, sufficient suppression should be done by system manufacturers.
- (8) Inserting or pulling I/F connectors causes any trouble when power supply and signal dates are on-state.I/F connectors should be inserted and pulled after power supply and signal dates are turned off.

9.5 Electrostatic discharge control

- (1) Since a TFT open cell consists of a TFT cell and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharge, persons who are handling a TFT open cell should be grounded through adequate methods such as a list band. Connector pins should not be touched directly with bare hands.
- (2) Protection film for a polarizer on a TFT open cell should be slowly peeled off so that the electrostatic charge can be minimized.

9.6 Precaution to strong light exposure

- (1) The TFT open cell should not be exposed under strong light. Otherwise, characteristics of a polarizer and color filter in a TFT open cell may be degraded.

9.7 Precaution to storage

When TFT open cells for replacement are stored for a long time, following precautions should be taken care of:

- (1) TFT open cells should be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during storage. TFT open cells should be stored at 0 to 35°C at normal humidity (60%RH or less).
- (2) The surface of polarizers should not come in contact with any other object. It is recommended that TFT open cells should be stored in the IPS Alpha Technology's shipping box.

9.8 Reliability

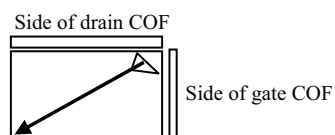
Since electronic components are implemented to this LCD, if water drops are adhered, it causes trouble. So, be careful of water drops adherence. (Especially around the driver circuit and the source PCB) If any problems or damages caused by water drops, etc. by any chance, these are not covered under warranty.

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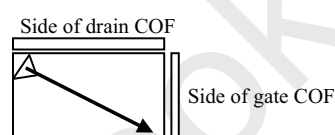
9.9 Precaution to handling protection film

- (1) The protection film for polarizers should be peeled off slowly and carefully by persons who are electrically grounded with adequate methods such as a list band. Besides, ionized air should be blown over during peeling action. Dusts on a polarizer should be blown off by an ionized nitrogen gun and so on.
- (2) The protection film should be peeling off without rubbing it to the polarizer. Because, if the film is rubbed together with the polarizer, since the film is attached to the polarizer with a small amount of adhesive, the adhesive may remain on a polarizer.
- (3) The TFT open cell with protection film should be stored on the conditions explained in 10.7 (1). However, in case that the storage time is too long, adhesive may remain on a polarizer even after a protection film is peeled off. Besides, in case that a TFT open cell is stored at higher temperature and/or higher humidity, adhesive may remain on a polarizer. The remained adhesive may cause non-uniformity of display image.
- (4) The adhesive can be removed easily with Normal-Hexane. The remained adhesive or its vestige on the polarizer should be wiped off with absorbent cotton or other soft materials such as chamois slightly contained Normal-Hexane.
- (5) The procedure of peeling protection film on pokarizer is recommended as follows.
 - (5-1)Set up LCD on the rest of the cell as the lower polarizer film comes on top gently.
 - (5-2)Peel off protection film from lower polarizer film with tape.

The protection film should be peeled as Drawing 1 or 2.



Drawing 1



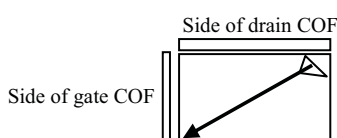
Drawing 2

(5-3)Set up LCD on the Backlight unit as the upper polarizer film comes on top gently.

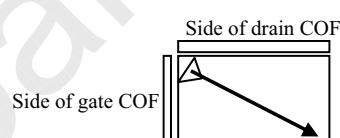
(5-4)Connect LCD surface to GND.

(5-5)Peel off protection film from upper polarizer film with tape.

The protection film should be peeled as Drawing 3 or 4.



Drawing 3



Drawing 4

9.10 Safety

- (1) Since a TFT cell is made of glass, handling to the broken TFT open cell should be taken care sufficiently in order not to be injured. Hands touched liquid crystal from a broken TFT open cell should be washed sufficiently.

9.11 Environmental protection

- (1) Flexible printed circuits and printed circuits board contain small amount of lead. Please follow local ordinance or regulations for its disposal.

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9.12 Use restrictions and limitations

- (1) This product is not authorized for use in life support devices or systems, military applications or other applications which pose a significant risk of personal injury.
- (2) In no event shall IPS Alpha Technology, Ltd., be liable for any incidental, indirect or consequential damages in connection with the installation or use of this product, even if informed of the possibility thereof in advance. These limitations apply to all causes of action in the aggregate, including without limitation breach of contract, breach of warranty, negligence, strict liability, misrepresentation and other torts.

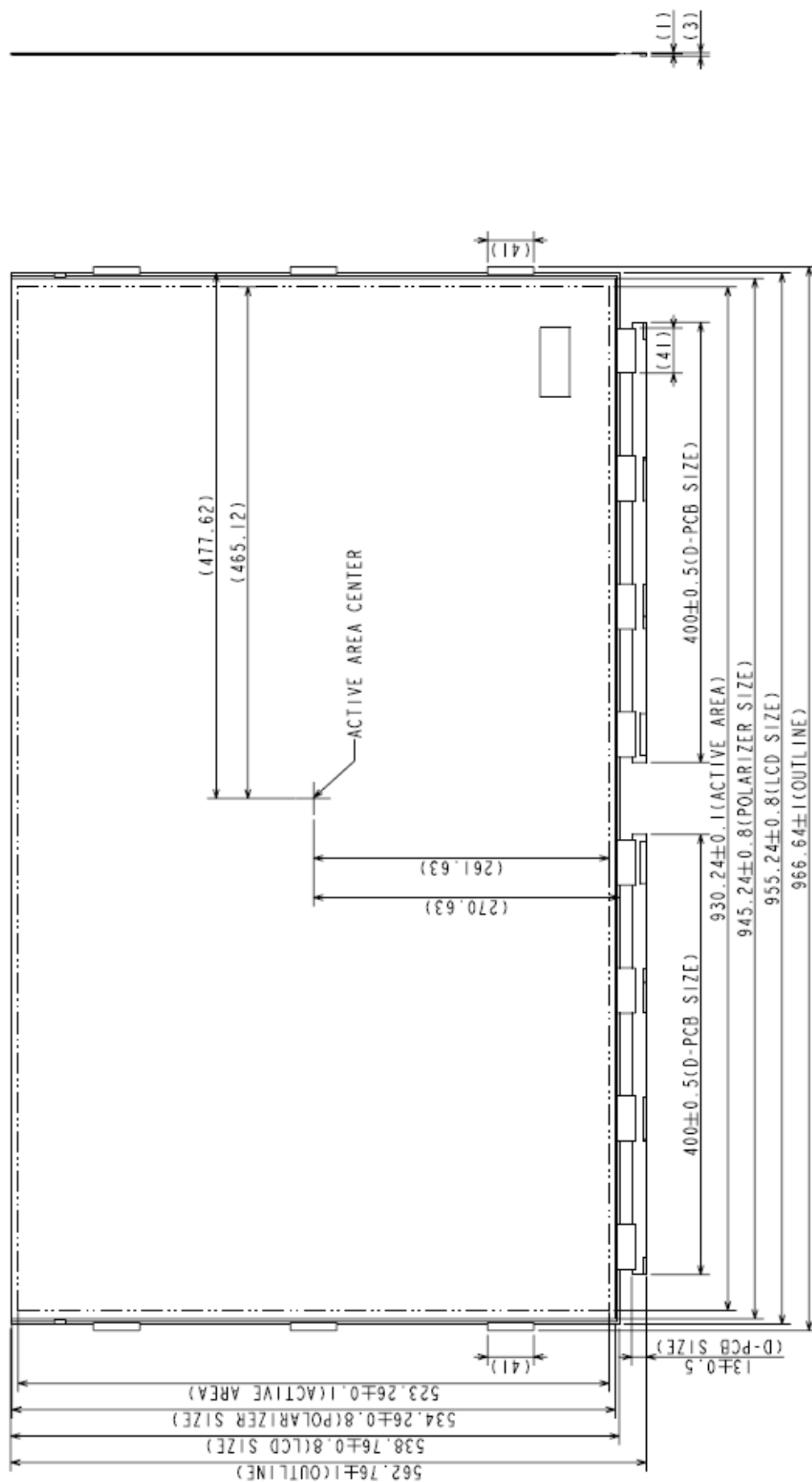
9.13 Others

- (1) Electrical components which may not affect electrical performance are subjective to change without notice because of their availability.

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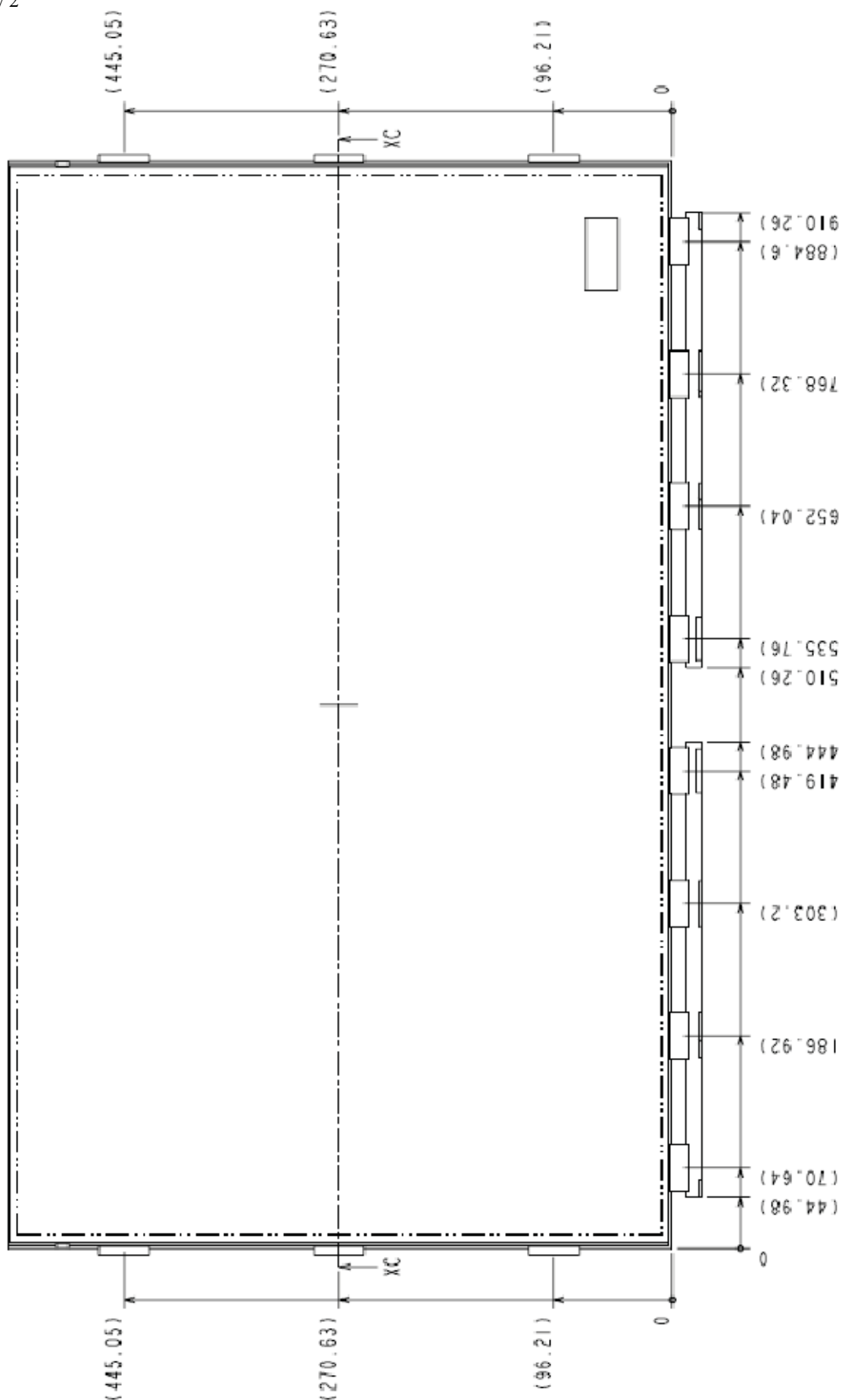
10. Dimensional Out Line

Front View 1



10. Dimensional Out Line

Front View 2





10. Dimensional Out Line

Front View 2

